

What Is Claimed Is:

1. A method for monitoring an execution of a program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller, comprising the steps of:

causing the debug logic to trigger an exception upon access to a specific address range during a program execution time;

causing the at least one microprocessor to configure the debug logic; and

causing the debug logic to execute an exception routine after the exception is triggered during the program execution time.

2. The method according to claim 1, wherein:

the exception corresponds to an interrupt of the execution of the program.

3. The method according to claim 1, wherein:

the debug logic is configured during a startup of the micro controller.

4. The method according to claim 1, further comprising the step of:

during the execution of the exception routine, performing the steps of:

resetting the micro controller,

starting up the micro controller again, and

initializing the program.

5. The method according to claim 4, further comprising the step of:

storing at least a type of a fault in a fault memory before the micro controller is reset and started up again and before the program is initialized.

6. The method according to claim 5, further comprising the step of:

storing a memory address that was accessed before an occurrence of the fault in the fault memory before the micro controller is reset and started up again and before the program is initialized.

7. The method according to claim 1, wherein:
the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time.
8. The method according to claim 7, wherein:
the debug logic monitors whether the program accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time.
9. The method according to claim 1, wherein:
the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory.
10. A control element for a micro controller, comprising:
an arrangement for storing a program, the program being executable on at least one microprocessor to perform the following:
causing a debug logic to trigger an exception upon access to a specific address range during a program execution time,
causing the at least one microprocessor to configure the debug logic, and
causing the debug logic to execute an exception routine after the exception is triggered during the program execution time.
11. The control element according to claim 10, wherein:
the control element corresponds to one of a read-only memory and a flash memory.
12. The control element according to claim 10, wherein:
the micro controller is arranged in a motor vehicle.

13. A micro controller, comprising:
at least one microprocessor;
a debug logic, wherein:
a program is executable on the at least one microprocessor,
the debug logic monitors an execution of the program during a program
execution time and triggers an exception upon access to a specific address range, and
the at least one microprocessor configures the debug logic; and
an arrangement for executing an exception routine after the exception is triggered
during the program execution time.
14. The micro controller according to claim 13, wherein:
the exception corresponds to an interrupt of the execution of the program.

13. A micro controller, comprising:
at least one microprocessor;
a debug logic, wherein:
a program is executable on the at least one microprocessor,
the debug logic monitors an execution of the program during a program
execution time and triggers an exception upon access to a specific address range, and
the at least one microprocessor configures the debug logic; and
an arrangement for executing an exception routine after the exception is triggered
during the program execution time.